SIDECAR Low-power control ASIC for focal plane arrays including A/D conversion and bias generation

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ABSTRACT

Large two-dimensional imaging arrays, spanning infrared focal plane arrays through visible CCDs, usually require extensive support electronics. We present an application specific integrated circuit (ASIC) that combines, on a single chip, all necessary functions to operate CMOS-based focal plane arrays and provide digital data from 12 to 16 bits. The interface to the external world is completely digital, thus eliminating the complexity of dealing with sensitive analog voltages. The ASIC's first application is for use with the HAWAII-2RG (a 2048 x 2048 multiplexer specifically optimized for the Next Generation Space Telescope). Due to its flexibility, it can control other FPAs and SCAs not requiring clocks or biases higher than 3.3 V. The low-power, system-on-chip controller comprises a 16-bit microcontroller, program and data memory, clock generator, bias generator, 36 programmable gain amplifiers (0 to 27 dB), thirty-six 12-bit 10 MHz A/D converters, thirty-six 16-bit 500 kHz A/D converters, glue logic and programmable I/O pads. When configured for NGST, we estimate ≤8.4 mW continuous power for the 2k×2k FPA and ASIC. The programmable ASIC, dubbed SIDECAR, for System for Image Digitization, Enhancement, Control And Retrieval, is likely an optimum "back-end" solution for other high-performance instruments.

Keywords: Infrared, Detectors, Focal Plane Array, Sensor Chip Assembly, Astronomy, ASIC

1. INTRODUCTION

In the 1970's, pioneering designers of infrared (IR) focal plane arrays strived to develop sophisticated imagers that ultimately proved especially difficult to produce. The nascent FPAs tried to use charge coupled device (CCD) technology for signal readout and exploited charge-based signal processing to enhance S/N ratio, manage dynamic range, mitigate the deficiencies of the then immature detectors, boost MTF, and enhance resolution. The available surface channel CCD processes ultimately did produce background-limited FPAs with high pixel operability at cryogenic temperatures, but largely without the most sophisticated signal processing bells and whistles.

By the mid-1980's, commercial CMOS matured to where state-of-the-art dynamic random access memory (DRAM) was migrating to 1.2 µm lithography. At the same time, 2 µm CMOS became available at significantly lower cost than was being incurred on specialized CCD production lines. This economic catalyst helped trigger the development of the first CMOS readouts for IR FPAs because the circuit densities were comparable to those available with CCD processes. By migrating to CMOS, high-density low-power amplification became available. The much larger pixel offset nonuniformity of the nascent CMOS readouts was not a major issue because the contemporary IR FPAs needed nonuniformity correction at that time. While the crude feature sizes precluded monolithic visible imagers, the resulting pixel pitches were compatible with infrared FPA development because the blur circle is an order of magnitude larger. Over the next two decades Moore's law [1] supplied the impetus for resurrecting on-chip signal processing.

Deep submicron CMOS technology is now enabling focal plane arrays (FPA) and sensor chip assemblies (SCA) with system-on-chip functionality. While imaging FPAs are making this transition as needed for visible and infrared applications, the changeover can be hastened by combining conventional FPAs with matching ASICs to control the sensor and provide clocks, biases and A/D conversion of the analog video stream. The resulting two-chip solution can be especially optimum for applications where the heat load on the cold finger must be minimized and compactness is preferred. Furthermore, it eliminates complex controller systems that can be huge, expensive and deplete valuable engineering resources.

Accordingly, we report our progress in exploiting deep sub-micron (≤0.25 μm) CMOS to produce advanced SCAs by developing an ASIC with system-on-chip integration. The ASIC can be collocated with the FPA on the cold finger or placed nearby. This solution helps mitigate instrument development issues such as low-noise handling of many video channels having relatively high characteristic impedance, routing many wires from the FPA to the electronics, and optimizing SCA heat load and load distribution. The resulting third-generation infrared SCAs provide compelling performance advantages with respect to sensitivity, spatial resolution, programmability, and noise immunity. Furthermore, they:

- enhance instrument functionality and capability while greatly reducing system bulk and power dissipation [2].
- provide localized A/D conversion that reduces the challenge of optimally engineering the complex transmission line between the sensor's analog circuits and the camera electronics
- facilitate on-demand sensor deployment to adeptly match each mission and ease logistics for operating sensors
- do not require elaborate camera electronics or months of system integration to achieve top performance

A major consequence is that new imaging cameras can rapidly "plug-and-play" an optimum sensor for a specific mission, or simultaneously support several sensors with differing capabilities on a common bus. In addition, high-performance infrared imaging is manageable at operating temperatures across the military temperature range to as low as 30K since the embedded digitizers dissipate low power up to 16 bits. When operated cryogenically, the CMOS-based support technology works better than at ambient temperature and hence can enable superior instrument performance than otherwise possible.

While the first application for the control ASIC is to help revolutionize astronomy via the Next Generation Space Telescope, it is compatible with many CMOS-based visible and infrared imaging sensors to produce a two-chip solution that makes obsolete an expensive rack of electronics. Since the integrated circuit can optimally distribute the development grief and risk throughout the camera (including the SCA) rather than simply overburdening the downstream electronics, we designate this first ASIC by the apt moniker SIDECAR, for System for Image Digitization, Enhancement, Control And Retrieval.

2. SIDECAR IC WITH SYSTEM-ON-CHIP INTEGRATION

Most contemporary FPA designs, including visible CCDs through infrared FPAs, focus on basic operation and are thus relatively crude with respect to their level of functional integration. Figure 1 shows that even clocks and biases are supplied to many conventional imaging sensors to generate analog video. Camera electronics subsequently digitize the video using commercial A/D converters. The result is a complex interface within the camera. The conventional imaging sensors include CCD-based and CMOS-based technologies. Practical issues stemming from the basic inability to optimally manage the high-resolution video signals, due to their high characteristic impedance, often degrade performance especially at frequencies above 5 MHz for 14-bit video and result in discrepancies between laboratory and system measurements of performance. While clocks and biases have been added to CMOS-based sensors over the past ten years, on-chip A/D conversion is not usually included for infrared sensors because low-power versions are not typically available for unencumbered cryogenic operation. Furthermore, the majority of generally available on-chip A/D converters typically provide ≤10 bits.

Combining an FPA with the SIDECAR ASIC results in the more optimal configuration of Figure 2. The resulting sensor chip assembly is self-contained, camera design is greatly simplified, and digital interface to the camera electronics is provided. The integration of such imaging system-on-chip technology to produce alternative 3rd generation IRFPAs hence represents a paradigm shift for emerging cameras, FLIR seekers and various imaging instruments if this alternative:

1. enhances performance
2. reduces overall camera complexity
3. maintains or reduces the total SCA power budget including the FPA and adjunct integrated circuit(s)
4. enables the development of sophisticated instruments that would otherwise be impractical.

The key development aspects for the SIDECAR IC involve optimizing low-noise management of high-resolution video signals having relatively high characteristic impedance, developing on-chip 12 to 16-bit digitization at very low power, enabling a smooth transition to using digital interface between the sensor and the camera electronics without adding noise on-chip or burning excess power, and successfully integrating the SoC functions. The key hurdles that must be overcome to supply the optimum solution for the NGST mission, for example, are discussed in this section.

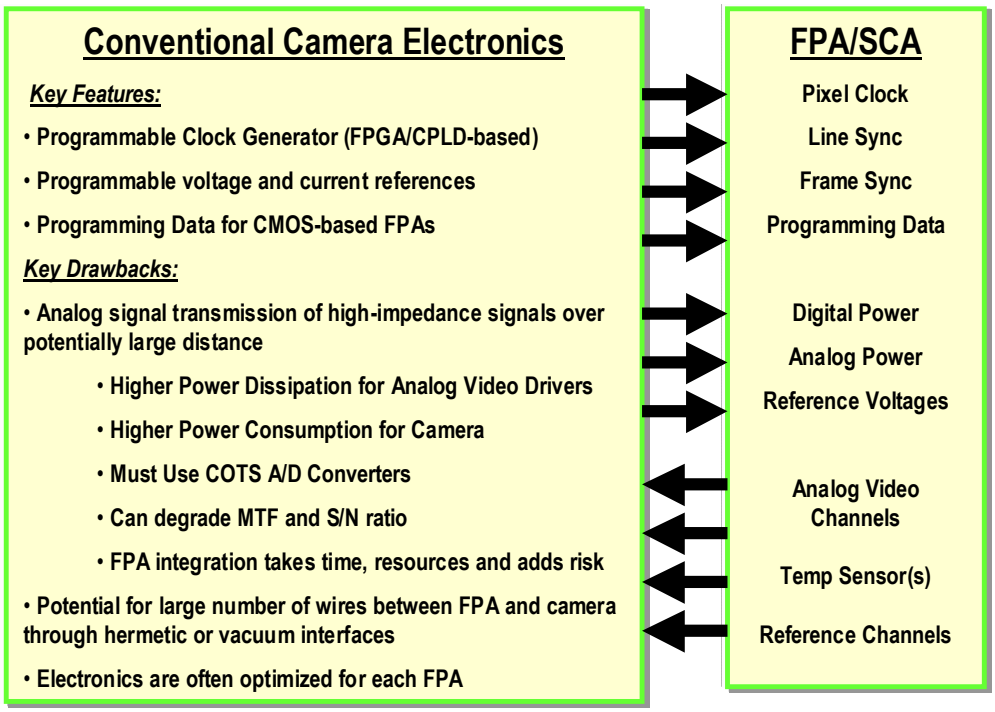


Figure 1. Functional distribution of camera with conventional FPA or SCA

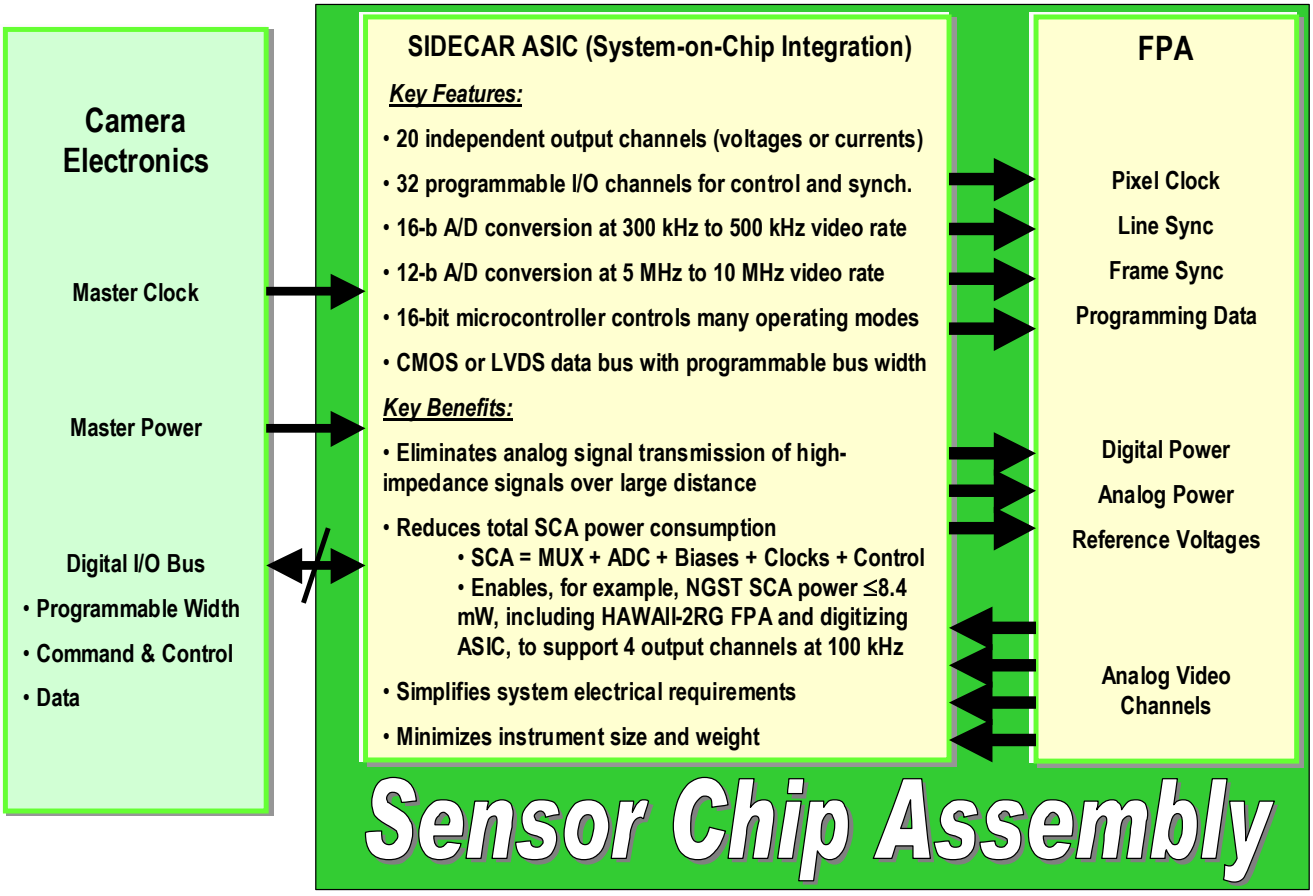


Figure 2. Functional distribution of camera with SCA comprising FPA and SIDECAR IC

Just as with stand-alone SoC sensors, complementing an FPA with the SIDECAR ASIC boosts capability while greatly reducing system bulk and power dissipation. Figure 3 epitomizes the resulting payoff by comparing two systems that produce digital video. On the left is an existing rack of electronics that produces ~12-bit digital video from a conventional 2nd generation infrared FPA with 32 analog outputs. On the right is a low-noise imaging system-on-chip sensor, specifically the ProCam-HD sensor [3], which directly provides ≥11-bit video via SoC functionality and programmability. The former consumes 400 Watts to generate 3.41 Gbps (14-bit digitization of the analog video from the 128 by 128 FPA at 15 kHz frame rate and <50 e- read noise). The latter consumes 0.25 W to generate ~1 Gbps (12-bit digitization from 1920 by 1088 FPA at 30 Hz frame rate and <30 e- read noise). Furthermore, the latter is compatible with chip-scale packaging. The actual vertical dimension of the chip-on-board package shown on the right is approximately one inch.

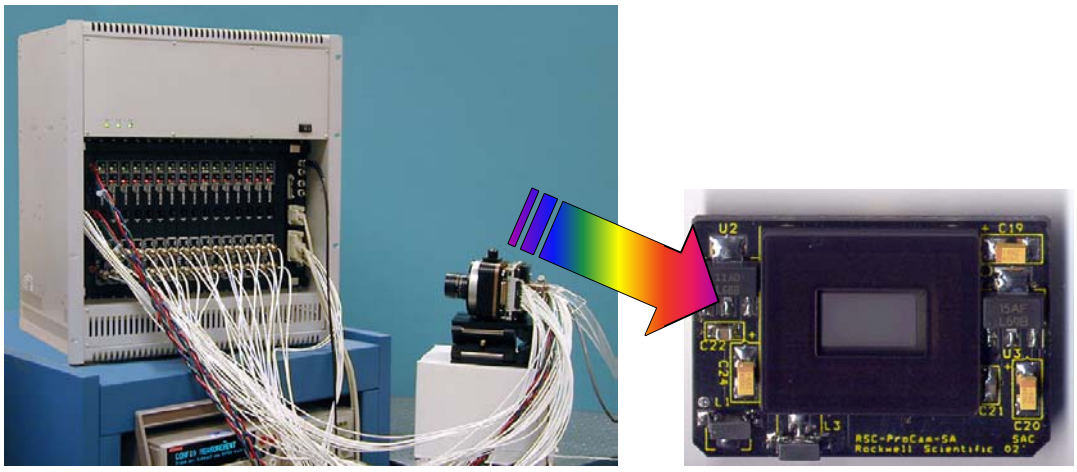


Figure 3. Payoff for migrating to System-on-Chip SoC or FPA with SIDECAR ASIC

2.1. SCA Optimization for the Next Generation Space Telescope: Power vs. Noise

Developing an optimum SCA for the Next Generation Space Telescope requires that the average total power dissipation for supplying 16-bit video at an aggregate video rate of 400 kHz must be ≤8.4 milliwatt. This is specification is very challenging, especially since instrument specifications mandate long cables for transmitting the video from the SCA.

Table 1 compares the settling time, noise and power for three candidate configurations to the specification we have flowed down from the NGST requirements. Two of the candidate embodiments are analog and a third is digital with low voltage differential signal (LVDS) configuration. To supply an analog signal, we assume that the FPA's output source follower drives both the cable and a preamplifier in the external electronics (Figure 4), the source follower current, I_{bias}, is optimized to achieve the maximum settling time, R_o is the corresponding output impedance for the FPA output buffer, R_c is the cable resistance (50 Ω/m for 5 meter cable), and C_c is the cable capacitance (33 pF/m; doubled in simulation due to possible second cable redundancy). The analog simulations showed that R_o ranges from 82 Ω to 385 Ω at cryogenic operating temperature for amplifier currents from 100 µA to 1000 µA and modeled transistor geometries (W/L) of 100/1, 200/0.7 and 400/0.5.

Table 1. Estimated noise, bandwidth and power budgets for analog and digital configurations

Video Configuration	Embodiment	Max Bandwidth or bit rate	Max time for settling (µs)	Maximum Noise	Peak Power	Total Operating Power
Flow-Down Specification	TBD: Optimum	100 kHz/tap or 2 MHz/18-b	Analog: 1.9	≤3.6 µV	-	1 mW average
Digital: LVDS	18 bits	2 MHz/18-b	-	±200,000 µV	38 µW/bit	18×38µW=684µW + ADC
Low Power Analog	4 taps	714 kHz/tap	3.1	≥3.6 µV	330 µW/tap	4×330µW=1.32mW
High-resolution Analog	4 taps	826 kHz/tap	1.6	≥3.6 µV	990 µW/tap	4×990µW=3.96mW

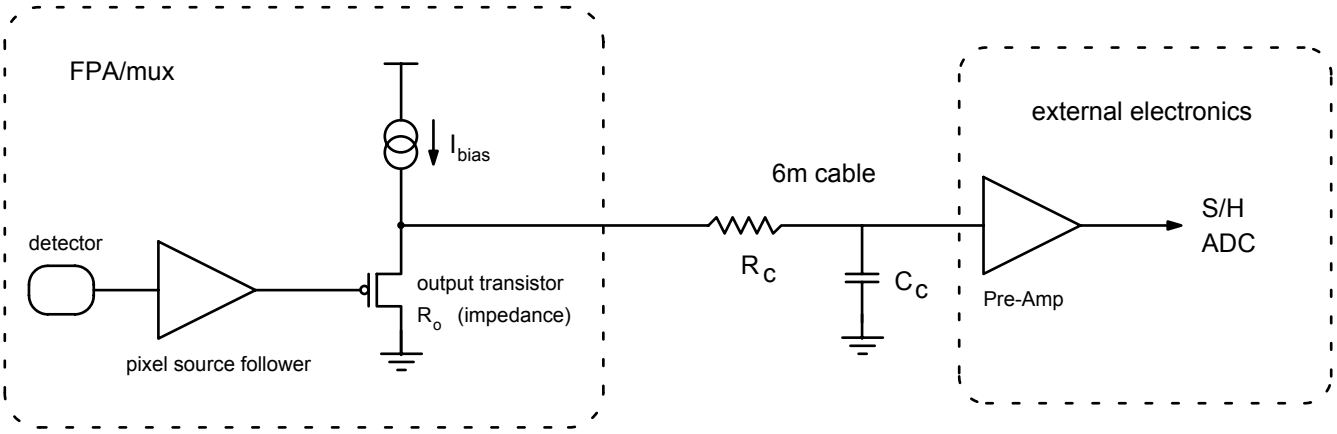


Figure 4. Candidate configuration for NGST analog video driver

Scrutiny of the table leads to several observations:

1. The digital configuration can greatly alleviate the challenge of achieving 16-bit performance and can meet the power budget if the ADC power can be minimized. The strongest argument for the ASIC solution is the fact that the transmission of sensitive analog signals over a long distance is eliminated.
2. The low power analog configuration will meet the power budget even at high readout duty cycles, where the duty cycle is the ratio of the readout time to the total time for readout and signal integration. However, this configuration's maximum settling time of 3.1 μs doesn't meet the flow-down specification of 1.9 μs even though its maximum bandwidth is 714 kHz. Further, the >4X larger bandwidth lowers the maximum noise spectral density from 9 nV/√Hz to an even more challenging 4.26 nV/√Hz {i.e., $3.6\mu V/(714\ kHz)^{1/2}$ }.
3. The high power analog configuration can meet the power budget at readout duty cycles of 25% or less, but its even larger maximum bandwidth imposes further burden on minimizing the composite noise spectral density—to below 4 nV/√Hz!

We thus conclude that NGST is best supported using a digital interface to the SCA, such as provided by the SIDECAR ASIC, even though this configuration adds the power from several 16-bit A/D converters to the total power budget. It is hence critical to minimize the power dissipation of the 16-bit A/D converters.

2.2. SCA Optimization for NGST: Low-Power A/D Conversion

As discussed above, a major development challenge for the SIDECAR ASIC is an ultra-low power A/D converter for digitizing 100 kHz video. The total power budget using digital I/O for the expected NGST configuration translates to per-channel goal of 1.2 mW per converter, which corresponds to A/D converter figure-of-merit of 0.18 pJ/LSB. This represents a significant advance in the state of the art (Figure 5) for low-power A/D conversion at 16-bit resolution, 100 ksps sampling rate, and commercial operating temperatures. We are therefore pursuing two schemes to minimize overall risk and are leveraging cryogenic operation to enhance efficiency at low risk. Our baseline approach (Approach 1) targets a maximum of 0.18 pJ/LSB. A backup scheme leverages the proven digitizing core from our ProCam-HD 12-b converter to conservatively target 0.2 pJ/LSB (Approach 2).

The ProCam-HD A/D converter has already advanced the state of the art for 12-bit A/D converter performance at 75 MHz and hence doubly serves as the basic digitizing engine for the 10 MHz A/D converter (Figure 6). The latter A/D converter implementation for SIDECAR targets a minimum efficiency of 0.05 pJ/LSB at 5 MHz. While this similarly represents significantly better power efficiency than previously demonstrated for A/D converters operated at commercial operating temperatures, cryogenic operation greatly reduces the risk of meeting our target. The FOM of 0.05 pJ/LSB represents power dissipation of only 1 mW at 100 ksps video rate.

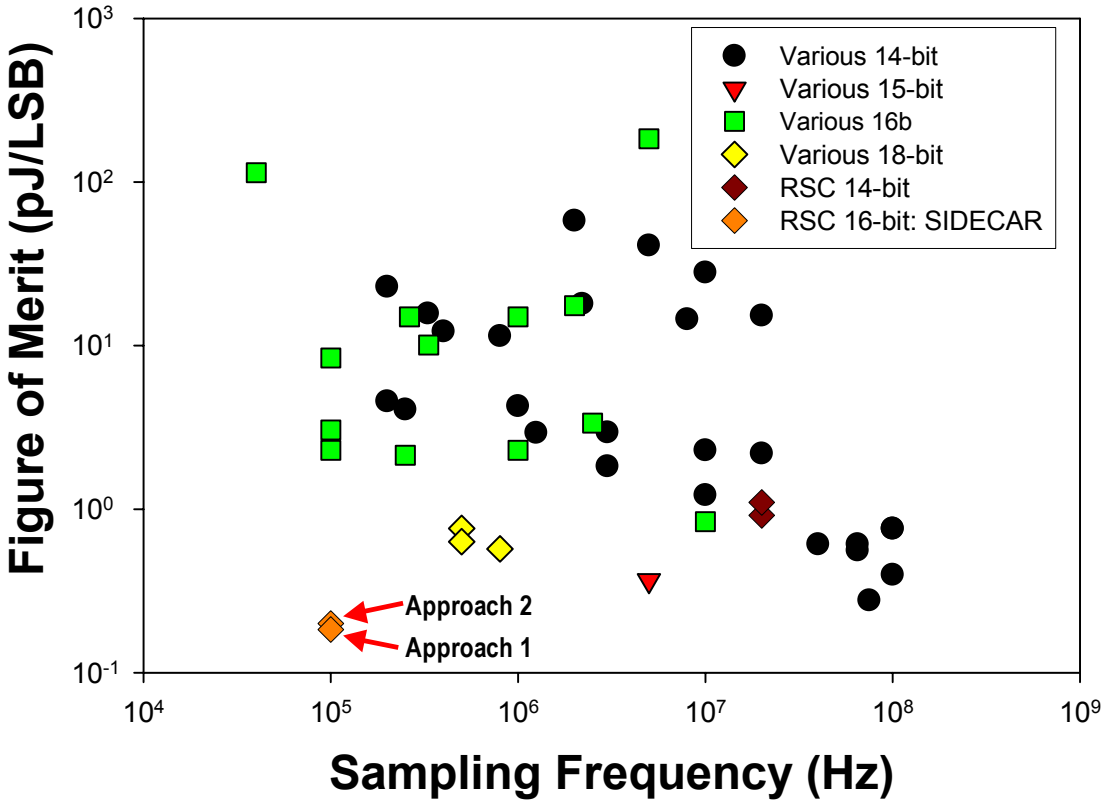


Figure 5. Figure of Merit (FOM) for efficiency of high resolution A/D converters vs. sampling frequency.

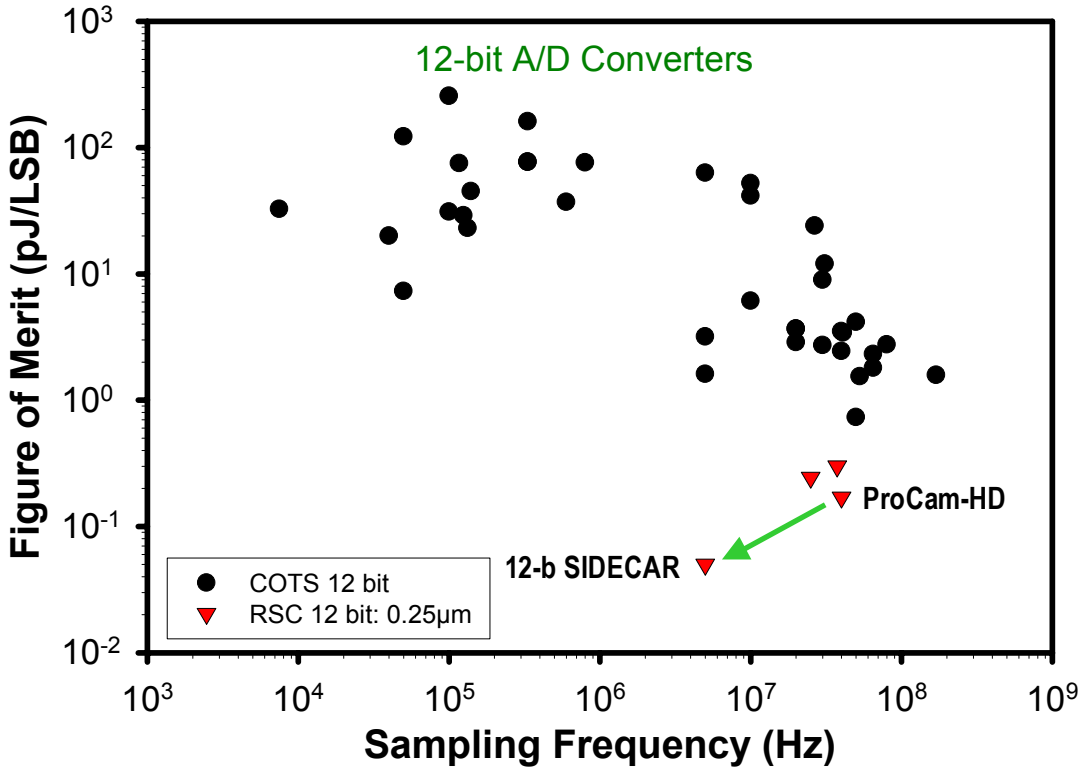


Figure 6. Figure of Merit (FOM) for efficiency of 12-bit A/D converters vs. sampling frequency.

3. ARCHITECTURE FOR SYSTEM-ON-CHIP SENSOR SIDECAR ASIC

The architecture of the SIDECAR ASIC comprises the following major blocks: analog bias generator, analog to digital converters, digital control and timing generation, data memory/processing, and digital data interface. To minimize development risk while exploiting both the system-on-chip functionalilty of ProCam-HD and the sophistication of the more conventional HAWAII-2RG [4-6] CMOS readout (2048^2 for visible and infrared astronomy), the NGST ASIC is leveraging ProCam-HD and 0.25µm CMOS via the derivative architecture shown in Figure 7 to:

- flexibly generate up to 20 channels of programmable analog references
- flexibly generate up to 32 channels of digital clocks and control signals
- flexibly provide 16-b A/D conversion of analog video at 100 kHz to 1 MHz video rate
- flexibly provide 12-b A/D conversion of analog video at 5 MHz to 20 MHz video rate
- flexibly control the various operating modes via 16-bit microcontroller
- eliminate analog signal transmission of high-impedance signals over large distance
- reduce the overall power consumption of the Sensor Chip Assembly (MUX + A/D converters + Bias Generation + Clock Generation)
- enable total power consumption of only 8.4 mW, including HAWAII-2RG FPA and 16-bit digitizing ASIC, to support 4 output channels at 100 kHz video rate
- simplify electrical requirements for the external system (via digital I/O)
- flexibly support CMOS or LVDS data bus with programmable bus width
- minimize size and weight of the resulting instrumentation

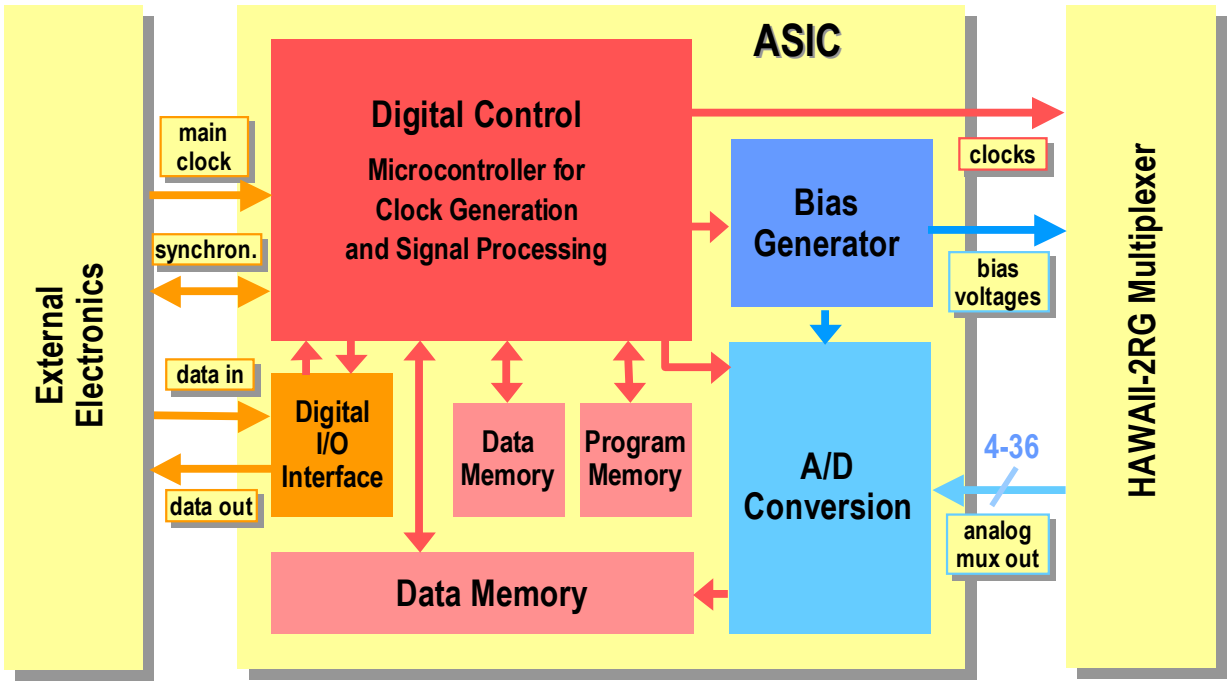


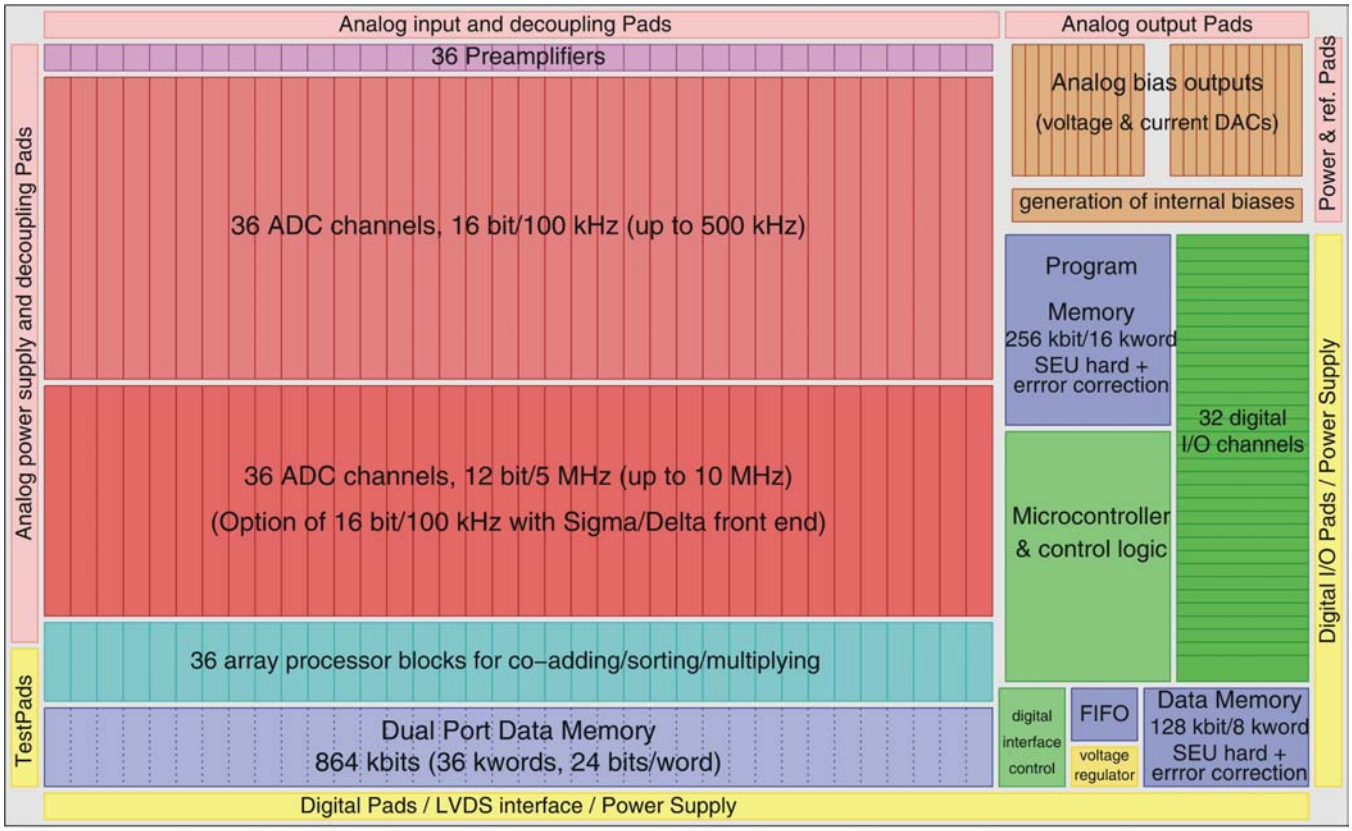
Figure 7. Sensor Chip Assembly for Astronomy: SIDECAR ASIC with HAWAII-2RG readout.

3.1. Floorplan and Operating Block Details

The SIDECAR ASIC has the following operating blocks that are situated per the floor plan shown in Figure 8:

- 16-bit RISC microcontroller with Harvard architecture and 3-stage pipeline
- 864 kbits of dual port data memory
- up to 256 kbits program memory (hardened for single event upset)
- 128 kbits of error-corrected data memory (hardened for single event upset)
- bandgap and externally-supplied reference voltage generation

- 36 channels of 16-bit A/D conversion at 100kHz to 1 MHz
- 36 channels of 12-bit A/D conversion at 5 MHz
- 20 reference channels (voltage and current) with 10-bit resolution
- 32 general purpose programmable I/O channels for ROIC control and synchronization
    - flexible pattern generator with programmable delays from 1 ns to 250 µs
- 1, 2, 4, 8 or 12-bit wide LVDS digital data bus to 200 Mbps
- 1, 2, 4, 8, 12, 16 or 24-bit wide CMOS digital data bus to 100 Mbps



total dimensions: 21mm x 13mm

Figure 8. SIDECAR ASIC floor plan.

The analog bias generator supplies 20 independent channels of programmable current and voltage sources. Each channel comprises a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength as illustrated in Figure 9.

To read out the analog signals from the visible or infrared FPA, the ASIC supports up to thirty-six analog input channels. Each input channel first provides a programmable gain amplifier having up to 27 dB of gain. This amplifier is also adjustable with respect to its bandwidth to allow for a tunable lowpass filter. The amplified and band-limited analog signals can then be optionally digitized by on-chip ADCs offering either 16-bit resolution at sample rates up to 500 kHz or 12 bit resolution at sample rates to 10 MHz. The four extra ADC analog input channels beyond the base of 32 support additional signals using similar signal chain to provide the best possible science. Additional FPA signals of the HAWAII-2RG include reference outputs to suppress common-mode signals using differential processing, window output for separately reading out the guide mode window, and temperature sensors.

A fully programmable and application optimized microcontroller is responsible for the overall ASIC control and for generating the specific timing patterns of the multiplexer clocks. A total of 32 digital I/O channels are available, which can be individually adjusted for driver strength and signal direction. Due to additional on-chip memory, simple data processing functions like pixel averaging or data sorting are possible. The microcontroller supports powerful arithmetic capabilities at maximum clock rate of ≥50 MHz using 16 kwords of program memory at 16 bits/word (on the ASIC, single event upset hardened, error code protected), 8 kwords of data memory (16 bits/word, single event upset hardened, error protected) and 32

kwords of data memory (24 bits/word, regular SRAM, can be used by the microcontroller and by special functions that provide simple arithmetic operations on all 36 channels in parallel (e.g. adding, shifting, multiplying).

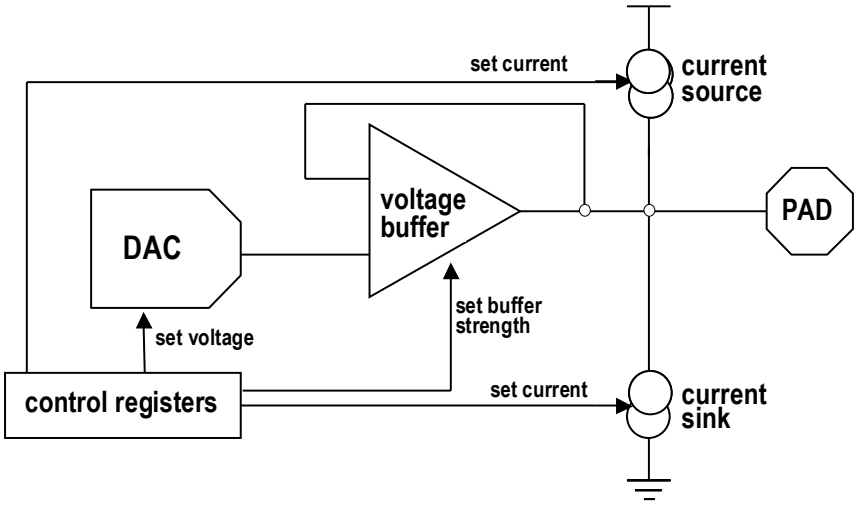


Figure 9. Architecture of programmable bias (voltage/current) reference outputs.

The microcontroller has two types of internal registers: standard (16 bits wide) and extended (24 bits wide). Most instructions affect only the 16 bit registers, but all arithmetic logic unit (ALU) operations also work with the 24 bit registers. The microcontroller supports about 110 different instructions including:

- Add
- Subtract
- add with carry, subtract with carry,
- average (add plus right shift in single cycle)
- multiply (16 x 16 integer and 24 x 16 pseudo-floating point)
- divide (16 x 16 integer and 24 x 16 pseudo-floating point)
- AND, OR, XOR, NOT, NEG
- shift left or right (arithmetic and logical)
- rotate left or right (with and without carry)
- set/reset/complement/test individual bits

All microcontroller instructions are single cycle, except the divide instruction may take up to 4 cycles depending on the clock speed. Program control instructions (jump, call, ret) can be 1, 2 or 3 cycles depending on the jump condition and the exact coding (due to pipeline architecture).

The SIDECAR ASIC has 24 output-interface that can be configured as either CMOS bus or LVDS bus. The former single-ended bus can be up to 24 bits wide; the latter supports up to 12-bit width since it is differential. This allows reading up to 36 on-chip 12 bit, 5 MHz ADCs at a CMOS speed of 100 MHz or an LVDS speed of 200 MHz. Various interface combinations are possible to facilitate lower bandwidth operation, e.g., NGST would use one single LVDS channel at ~10 Mbits/sec.

Finally, a serial data interface is implemented to read the digitized pixel values and program the ASIC. The interface protocol is custom to reduce risk and also to make SIDECAR adaptable to many different applications. It is fairly simple to build a board that communicates with the ASIC by using a newer generation FPGA, e.g., Xilinx. Such boards provide sufficient speed and infrastructure (LVDS ports, DLLs, etc.) to support all of the ASIC readout modes.

The ASIC is programmed via its DataIn and MasterClock inputs. The synchronous relationship between DataIn and MasterClock is shown in Figure 10. To program the sensor, DataIn comprises:

- 20 bits per cycle including
    - one start bit (1), one stop bit (0), one parity bit
    - 16 data bits
    - 1 address bit which indicates single word or block transfer
- block transfer of up to 256 words per package, uses header and checksum

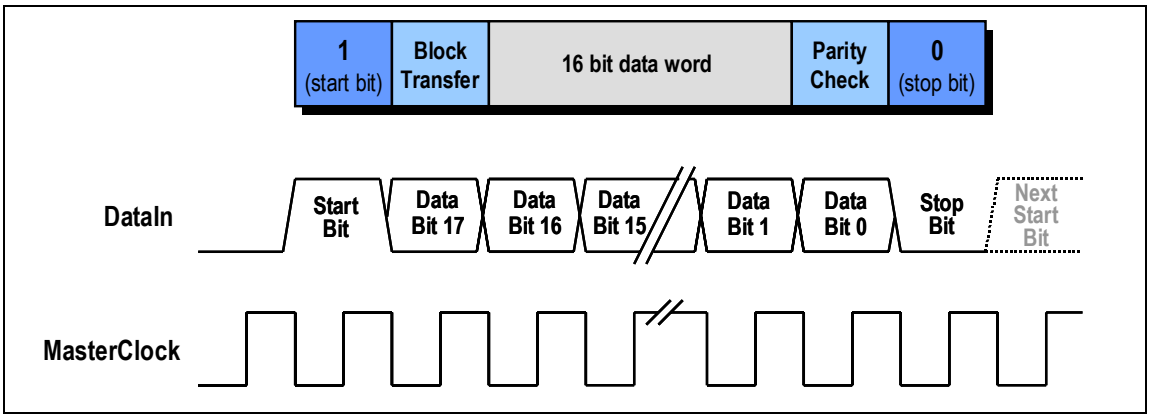


Figure 10. Programming sensor: DataIn and MasterClock

Imaging data is similarly received from the ASIC as per Figure 11, which shows the synchronous relationship between DataOut and MasterClock. To read the imaging data from the sensor, DataOut comprises:

- 20-28 bits per cycle
  - one start bit (0), one stop bit (1), one parity bit
  - 16-24 data bits
  - 1 additional bit to indicate certain conditions
- block transfer of up to 2048 pixels per package, uses header and CRC checksum

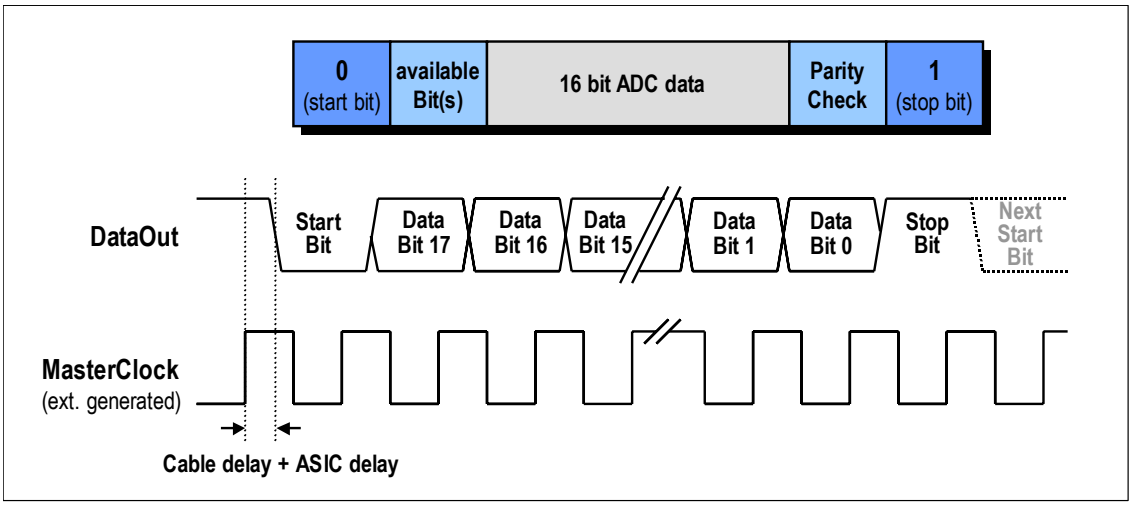


Figure 11. Reading imaging data from sensor: DataOut and MasterClock

4. ASIC INTERFACE DESCRIPTION EXAMPLE: NGST

The SIDECAR ASIC provides all the necessary clocks and biases to run the HAWAII-2RG ROIC. When packaged as a 4k by 4k mosaic using four HAWAII-2RG FPAs, 4 SIDECAR ASICs, the resulting NGST SCA assembly is shown in Figure 12. The SIDECAR ASICs are not visible in this top view as they are mounted on the underside of the package.

Figure 12. 4k by 4k mosaic comprising four HAWAII-2RG IRFPAs, four SIDECAR ASICs and cables

Figure 13 shows the electrical interface among each HAWAII-2RG IRFPA, its supporting ASIC and the sensor control electronics (SCE) in the main instrument. The SCE provides one master clock and one data line to program the ASIC. The SCE will also supply one stable reference DC voltage, although the ASIC optionally provides the reference internally from a bandgap reference or V_{dd}. While the ASIC supports up to 36 analog inputs with two ADC options, the NGST mission calls for using a minimum four inputs. The extra ADC analog input channels support additional signals including, e.g., the reference output, window output, and temperature sensors.

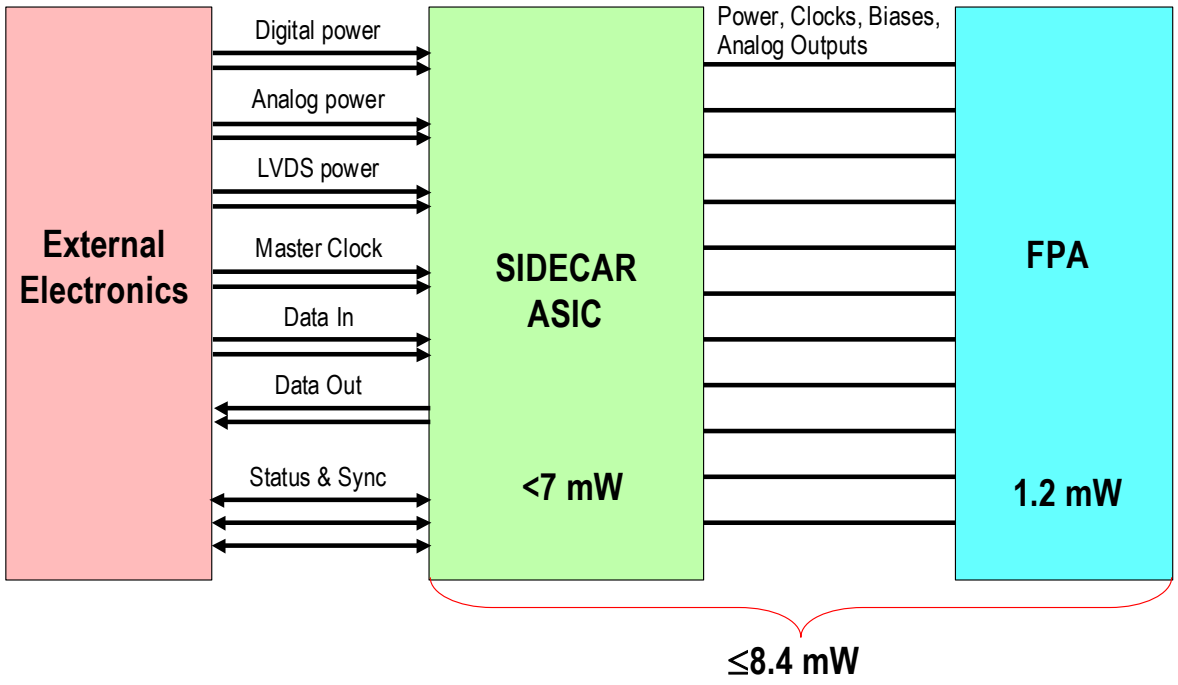


Figure 13. ASIC Interface to Hawaii-2RG IRFPA and Sensor Control Electronics (SCE)

As noted in the preceding figure, the total NGST-specific power dissipation for the combination of the HAWAII-2RG IRFPA and the SIDECAR ASIC is a minimum of ≤8.4 mW using the optimized LVDS serial interface to program the SCA and read the imaging data. The power budget breakdown is listed in Table 2.

Table 2. Estimated Power Budget for NGST Operation: SIDECAR + HAWAII-2RG

Subblock	Power consumption per output	Total power consumption
HAWAII-2RG	300 µW	1.2 mW
ADC	1.3 mW (goal)	5.2 mW
ADC	0.6 mW	0.6 mW
Microcontroller & Clocking	1.0 mW	1.0 mW
Serial Interface: LVDS (standard) LVDS (optimized) CMOS (2 MHz, 200 pF, 2.5 V) CMOS (2 MHz, 200 pF, 1.0 V)	 750 µW 250 µW 600 µW 100 µW	 3.0 mW 1.0 mW 2.4 mW 0.4 mW
Total (minimum)	**1.7 mW** (+ 1.6 mW offset)	**8.4 mW**

5. SUMMARY AND CONCLUSIONS

While RSC's latest FPAs and sensor chip assemblies (SCA) are complete low-power imaging systems-on-chip (i-SoC) in hybrid and monolithic configurations that provide digital video at ≥12 bits for 3rd generation infrared and visible cameras, we are also developing a full-featured ASIC to enable producing very large high-performance mosaic SCAs for next-generation instruments including telescope sensors and to complement conventional FPA designs. The programmable ASIC, dubbed SIDECAR, is likely an optimum "back-end" solution for other high-performance instruments even though it is optimized for the Next Generation Space Telescope. The low-power, system-on-chip controller comprises a 16-bit microcontroller, program and data memory, clock generator, bias generator, thirty-six 12-bit 5 MHz A/D converters, thirty-six 16-bit 100 kHz A/D converters, glue logic and programmable I/O pads. When programmed to optimally meet the NGST requirement, the predicted total power of the 2k x 2k FPA and the NGST ASIC, including clocks, biases, control and digitization, is ≤8.4 mW.

RSC is hence developing an ASIC to quickly leverage this paradigm shift. We expect to received completed wafers from the 1st fabrication lot by the end of 2002. While the ASIC's design works optimally with the HAWAII-2RG readout, its high degree of programmability will allow its use with a variety of infrared and visible FPAs to assemble SCAs that operate from room temperature to cryogenic temperature. Such a hybrid multi-chip SCA allows instrument designers to:

- simplify the overall system architecture and use fewer wires
- eliminate the risks and problems of transmitting low-noise analog signals over a long distance
- reduce the risk of integrating one or more FPAs to build abutted mosaics
- offer high flexibility and redundancy due to broad programmability
- significantly reduce the overall system power consumption
- gather 16-bit images at ≤500 kHz (1 tap) to 9.6 MHz (32 taps) or 12-bit images at ≤10 MHz to maximum aggregate video rate of 160 MHz

Clearing these hurdles likely eliminates the discontinuity that is typically seen today between idealized laboratory and practical systems measurements.

6. ACKNOWLEDGMENTS

The authors gratefully acknowledge the sponsorship of NASA for funding the development of the HAWAII-2RG focal plane array. We also deeply appreciate their enthusiastic feedback regarding our developing the SIDECAR ASIC. Finally, we are thankful for the development funding and management support provided jointly by Rockwell Scientific Company and the Institute for Astronomy at the University of Hawaii; our goal is to help enable the best possible science in high-performance imaging instruments such as the Next Generation Space Telescope. Otherwise our developing the SIDECAR ASIC would not have been possible.

7. REFERENCES

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